DATA SHEET

Power Your Critical Mission Today

# VSCPL0510SG SERIES

## RADIATION TOLERANT DC-DC CONVERTERS




VSCPL0510SG - Exact marking may differ from that shown

| Models Available |
|---|
| Input Range: 4.5 V to 6 V |
| Output Range: 0.6 V to 3.6 V, 10A |
| Wattage: up to 36 W |

## 1.0 DESCRIPTION

The VSCPL0510SG Series is a commercial off the shelf DC-DC converter designed for the 'NewSpace' market. Performance is guaranteed through the use of radiation lot acceptance tested (RLAT) components. Our proprietary packaging creates a dual side heatsinking option with very low outgassing. The surface mount design enables streamlined reflow soldering alongside other SMT components for simplified board-level integration.

Radiation tested to 42 MeV/mg/cm² with no destructive SEE events (SEGR, SEB, and SEL) and tested to 40 krad(Si), guaranteed to 30 krad(Si), for TID in accordance with VPT's inhouse radiation hardness assurance (RHA) plan.

The VSCPL0510SG Series is designed for smaller satellites in low earth orbits (LEO), and NASA Class D missions where the balance of cost and guaranteed performance is critical.

## 1.1 FEATURES

- Operates from 4.5 – 6 V input
- Adjustable Output from 0.6 – 3.6 V
- Up to 10 Amps Output
- Peak efficiency up to 95%
- Output Inhibit Control
- Low Output Noise
- Short Circuit Protection
- Synchronizable to an external clock
- Continuous operation over the full temperature range of -55 °C to +105 °C with no power derating
- Surface-mount design for simplified production.

## 1.2 SPACE LEVEL CHARACTERIZATIONS

- Guaranteed TID performance to 30 krad(Si) including LDR
- SEE tested to 42 MeV/mg/cm². Transients are fully analyzed for cross-section and magnitude at 30 MeV/mg/cm²
- Radiation Hardness Assurance, see Section 6.5 herein
- Mean Time Between Failures (MTBF) calculations available
- Failure In Time (FIT) numbers available

## 1.3 MANUFACTURING AND COMPLIANCE

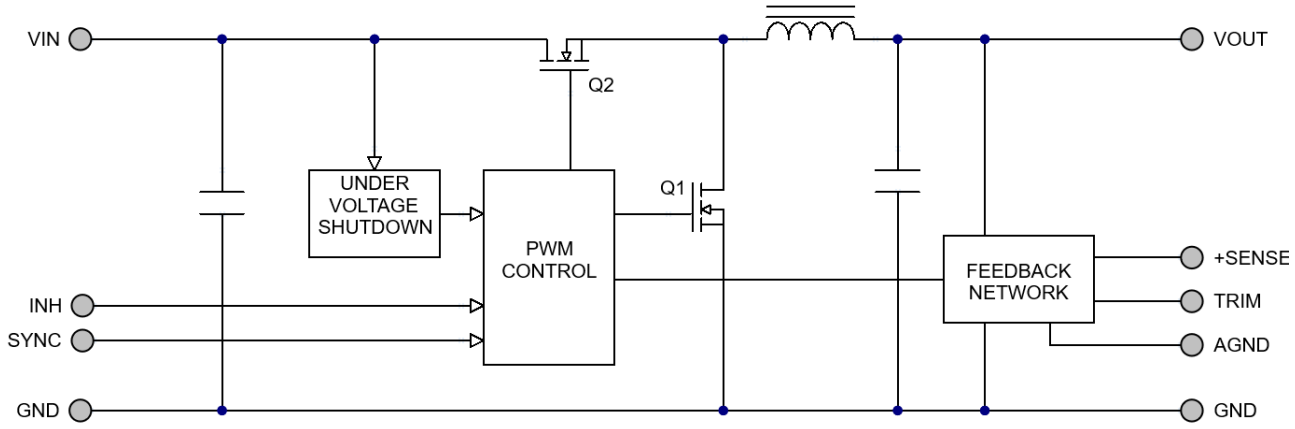
- Manufactured in an ISO9001, J-STD-001, and IPC-A-610 certified facility.

## 1.4 PACKAGING

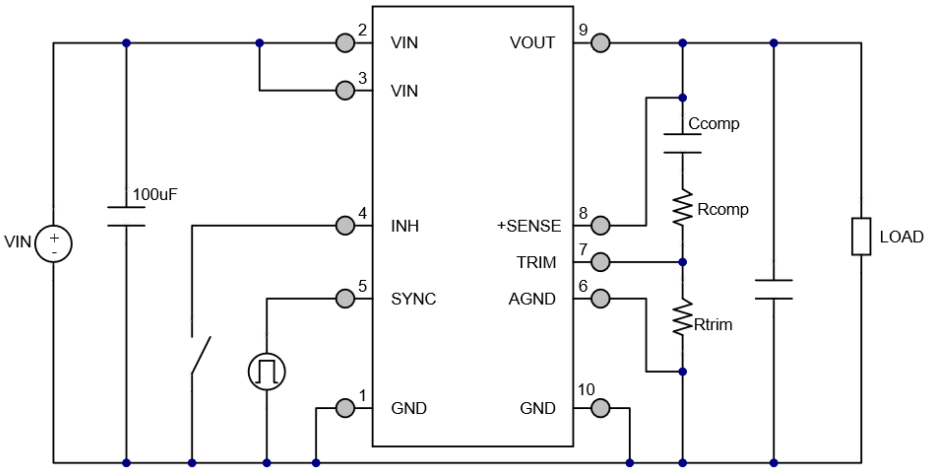
- Low-profile: 0.82" x 0.87" x 0.30"
- Max weight: 12 g

## 2.0 DIAGRAMS

### 2.1 BLOCK DIAGRAM




### 2.2 CONNECTION DIAGRAM




1. Rtrim should be connected directly across pins 7 and 6 as close as possible to the VSCPL.
2. AGND should be connected to GND close to the VSCPL. Voltage difference between the AGND and the GND pins greater than 0.3 V may result in regulation error and/or damage to the VSCPL.
3. If not using INH, leave pin 4 open.
4. If not using SYNC, leave pin 5 open or connected to GND.
5. Rcomp and Ccomp form part of the converter's compensation network. See Section 6.2.4 for guidelines on selecting values.

## 3.0 SPECIFICATIONS

## 3.1 ABSOLUTE MAXIMUM RATINGS

| Absolute Maximum Ratings | | | |
|---|---|---|---|
| Input Voltage (Continuous): | -0.5 V to 6 V | Operating Temperature (Full Load): | -55 °C to +105 °C |
| Input Voltage (Transient, 1 second): | -0.5 V to 7 V | Storage Temperature: | -55 °C to +125 °C |
| AGND | -0.3 V to 0.3 V | Lead Solder Temperature (10 seconds): | 300 °C |

## 3.2 PERFORMANCE SPECIFICATIONS

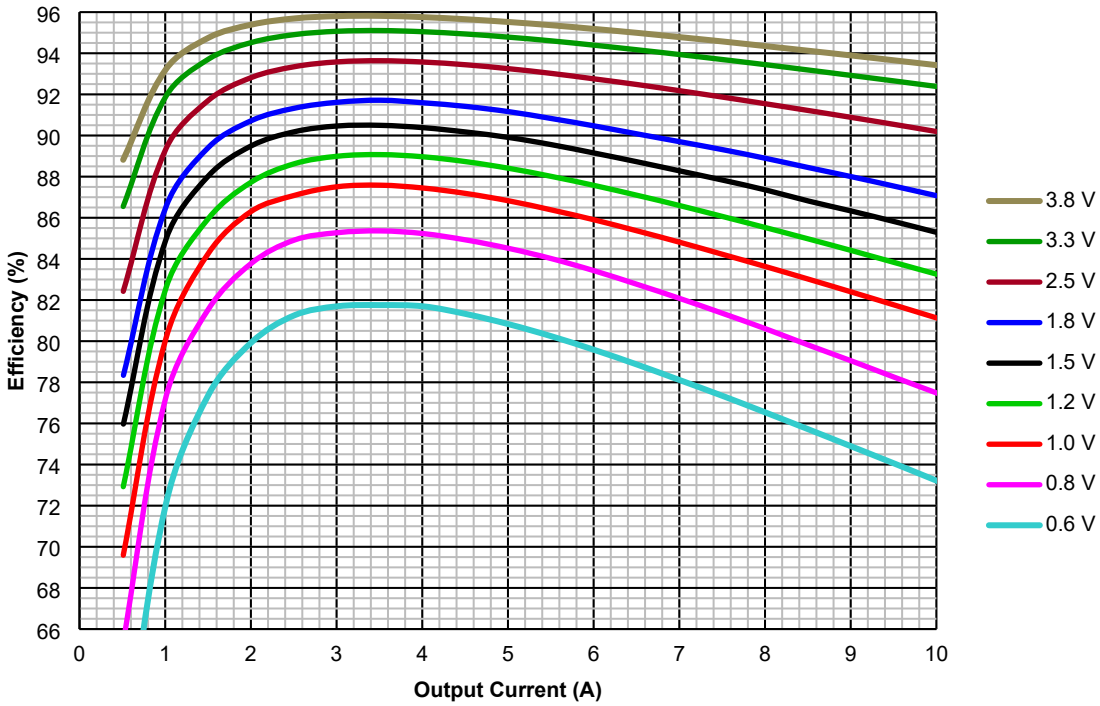
Tcase = -55 °C to +105 °C, Vin = +5 V ± 5%, Full Load, Unless Otherwise Specified

| | | VSCPL0510SG | | | |
|---|---|---|---|---|---|
| **Parameter** | **Conditions**[1] | **Min** | **Typ** | **Max** | **Units** |
| **INPUT** | | | | | |
| Voltage[2] | Continuous | 4.5 | - | 6 | V |
| Current | INH = GND | - | 24 | 40 | mA |
| | Vout = 3.3V, No Load | - | 55 | 150 | mA |
| Undervoltage Lockout[2,3] | Turn-On | 4 | 4.3 | 4.45 | V |
| | Turn-Off | 3 | 3.5 | 3.8 | V |
| **OUTPUT STATIC** | | | | | |
| Voltage | Tcase = 25 °C | -1.0 | - | +1.0 | %Vout |
| | Tcase = -55 °C to +105 °C | -1.5 | - | +1.5 | %Vout |
| Power[4] | | 0 | - | 36 | W |
| Current | Continuous | 0 | - | 10 | A |
| Ripple Voltage | Vout = 0.8 V to 3.3 V, 20 Hz to 10 MHz | - | 25 | 100 | mVpp |
| Load Regulation | No Load to Full Load | - | 0 | 0.2 | % |
| Short Circuit Power Dissipation | Vout = 3.3 V prior to short circuit | - | 0.5 | 2 | W |
| **OUTPUT DYNAMIC** | | | | | |
| Load Step, Half to Full Load | Output Transient, Vout = 3.3 V | - | 100 | 140 | mVpk |
| | Recovery[5] , Vout = 3.3 V | - | 30 | 120 | µs |
| Turn-On, Vin = 0 V to 5 V | Delay | - | 8 | 10 | ms |
| | Overshoot | - | 0 | 15 | mVpk |
| **FUNCTION** | | | | | |
| INH Pin Input[2] | Output Inhibited | 0 | - | 0.3 | V |
| INH Pin Open Circuit Voltage[2] | Output Enabled | - | 1.4 | 2.5 | V |
| SYNC Frequency Range | $V_H$ - $V_L$ = 5 V, D = 20-80% | 250 | - | 300 | kHz |
| **GENERAL** | | | | | |
| Efficiency, Full Load | Vout = 3.3V | 89 | 92 | - | % |
| Capacitive Load[2] | Vout ≤ 2 V | - | - | 5000 | µF |
| | Vout ≥ 2 V | - | - | $\frac{10000}{Vout}$ | µF |
| Switching Frequency | | 200 | 250 | 300 | kHz |
| Weight | | - | - | 12 | g |
| MTBF (MIL-HDBK-217F) | SF @ Tcase = 55 °C | - | 26.5 | - | MHr |
| **POST-RAD LIMITS**[6] | | | | | |
| Output Voltage | Tcase = -55 °C to +105 °C | -2.0 | - | +2.0 | %Vout |

1. Performance specifications are guaranteed with 100 µF from VIN to GND and Rcomp = 20 Ω, Ccomp = 2.7 nF.
2. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.
3. Output voltage not necessarily in regulation.
4. Dependent on output voltage.
5. Time for output voltage to settle within 1% of steady-state value.
6. Post-RAD limits are within standard limits except where noted.

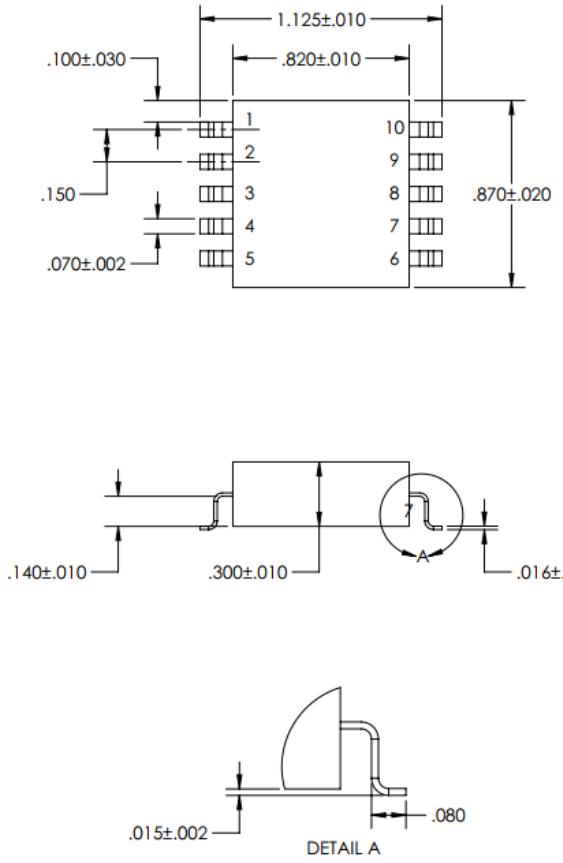
## 4.0 PERFORMANCE CURVES

### 4.1.1 VSCPL0510SG Efficiency (Typical, 25 °C, Vin=5V)



## 5.0 MECHANICAL OUTLINES AND PINOUT

**Standard Package Option:**




1. Tolerances are ±0.005" unless otherwise stated.
2. Case temperature is measured on the center of the baseplate surface on the underside of the converter.
3. Materials: Body (Epoxy); Pin (Copper, alloy 110, gold over nickel plating).

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | GND | 6 | AGND |
| 2 | VIN | 7 | TRIM |
| 3 | VIN | 8 | +SENSE |
| 4 | INHIBIT | 9 | VOUT |
| 5 | SYNC | 10 | GND |

## 6.0 TECHNICAL NOTES

Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

## 6.1 GENERAL INFORMATION

### 6.1.1 Topology Description

The VSCPL0510SG is a non-isolated, fixed-frequency, radiation-tolerant, synchronous buck converter. It operates from a 4.5 V to 6 V input range and provides a stepped-down, precisely regulated, programmable output voltage at high efficiency. The VSCPL0510SG is optimized for low voltage point-of-load (POL) applications.

### 6.1.2 External Components

The VSCPL0510SG Series has internal input and output capacitors. To meet the performance specifications in Section 3.2, a minimum additional 100 µF tantalum input decoupling capacitor is required. The VSCPL0510SG is stable with no load capacitance. Additional output capacitance is allowed up to the maximum listed in Section 3.2. An external resistor across the TRIM and AGND pins set the output voltage. The output voltage defaults to 0.6 V if no resistor is used. A series RC network must be placed across the +SENSE and TRIM pins in order to provide compensation to the converter's control loop. Section 6.2.4 gives guidelines for selecting values.

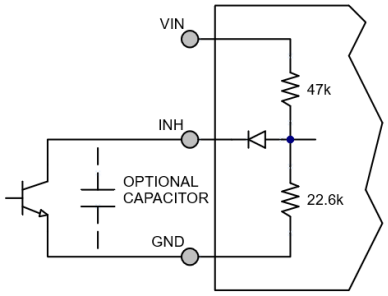
### 6.1.3 Source Impedance

The impedance of the input source can interact with the POL converter and impact performance. High source impedance is often caused by a long input cable or other components added in series with the input. In some cases, additional input capacitance will be needed to stabilize the system.

## 6.2 FUNCTION DESCRIPTIONS

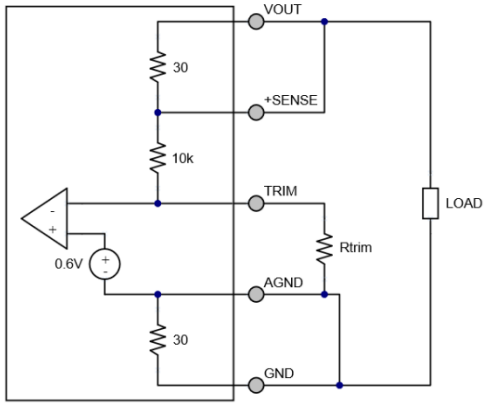
### 6.2.1 On/Off Control (Inhibit)

The INH (Inhibit) pin is a control pin referenced to GND. The INH pin must be driven using an open collector or open drain configuration. Pulling the INH pin low disables the converter output. Leaving INH open enables the output, allowing the converter to operate normally. The pin must be pulled below 0.3 V to disable the output. An optional capacitor from INH to GND may be used to delay turn-on. The INH pin should be left open if not used.




### 6.2.2 Adjusting the Output Voltage (TRIM)

The output voltage of the converter is set with an external resistor connected from the TRIM pin to the AGND pin. Use the equations or table below to choose the trim resistor value. Choose the next closest standard resistor value. Greater precision for non-standard Trim resistor values can be obtained using a parallel combination of standard resistors. A trim resistor tolerance of 0.1% is recommended to achieve an accurate output voltage. The default output voltage with the TRIM pin left open is 0.6 V.




$$R_{TRIM} = \frac{6000\Omega}{V_{OUT} - 0.6V}$$

$$V_{OUT} = \frac{6000\ \Omega}{R_{TRIM}} + 0.6\ V$$

| VSCPL0510SG | | |
|---|---|---|
| **+Vout (V)** | **Rtrim (Ω)** | **Parallel Combination (Ω)** |
| 0.6 | Open | - |
| 0.8 | 30k | - |
| 0.9 | 20k | - |
| 1.0 | 15k | - |
| 1.2 | 10k | - |
| 1.5 | 6.6667k | 10k \|\| 20k -or- 12k \|\| 15k |
| 1.8 | 5k | 10k \|\| 10k -or- 7.5k \|\| 15k |
| 2.0 | 4.2857k | 7.5k \|\| 10k |
| 2.5 | 3.1579k | 3.16k \|\| 4750k |
| 2.8 | 2.7273k | 3k \|\| 30k -or- 2.8k \|\| 105k |
| 3.0 | 2.5k | 3k \|\| 15k |
| 3.3 | 2.2222k | 2.4k \|\| 30k |
| 3.4 | 2.14289k | 2.4k \|\| 20k |
| 3.5 | 2.06897k | 2.4k \|\| 15k |
| 3.6 | 2k | - |
| 3.7 | 1.93548k | 2.4k \|\| 10k |
| 3.8 | 1.875k | 2k \|\| 30k |
| 3.9 | 1.8182k | 2k \|\| 20k |
| 4.0 | 1.76471k | 2k \|\| 15k |

The VSCPL0510 is fully specified for an output voltage of 0.6 V to 3.6 V at 10 A output current for the entire input voltage range of 4.5 V to 6 V. Higher output voltages are possible if the input voltage range or output current is restricted, and the transient response and regulation may worsen at low line due to duty cycle saturation. The line impedance may also affect the maximum achievable output voltage under load. The minimum input voltage should be at least 1.25 times the output voltage to have good transient response and load regulation at the full 10 A output current.

### 6.2.3 Output Capacitors

Output capacitors for point-of-load (POL) DC/DC converters should be chosen to meet output voltage ripple and transient requirements. Meeting the transient response requirement is accomplished by making the output impedance of the converter sufficiently small. Given the high control bandwidth of POL converters like the VSCPL series, the peak output impedance is typically dominated by the equivalent series resistance (ESR) of the bulk output capacitance. Therefore, the output capacitors should be chosen to set a certain maximum total ESR. The total ESR is the parallel combination of the internal bulk capacitor's ESR and that of the added capacitors. Given the output voltage transient requirement, maximum load step, and the ESR of each bulk capacitor that will be added, the number of added capacitors needed is calculated with the following equations:

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}}$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}}$$

| Parameter | Definition |
|---|---|
| $\Delta V_{OUT}$ | Max $V_{OUT}$ transient allowed |
| $\Delta I_{OUT}$ | Max load current step |
| $ESR_{TOTAL}$ | Total combined parallel ESR, including internal and added capacitors |
| $ESR_{ADDED}$ | Combined parallel ESR of the added capacitors |
| $ESR_{INTERNAL}$ | ESR of the internal bulk capacitor (**13.11 mΩ max** under worst-case conditions) |
| $ESR_{EACH}$ | ESR of each of the added capacitors |
| N | Number of added capacitors |

Make sure that the added capacitance does not violate the maximum allowed output capacitance using the following equation (up to 5000µF):

$$C_{OUT-MAX} = \frac{10000\mu F}{V_{OUT}}$$

For example, assume that $V_{OUT}$ is 2.5 V, the maximum output transient allowed is 37.5mV, and the load step is 4.5 A. Assume the output capacitors being used are 330 µF and have a maximum ESR of 50 mΩ each.

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{37.5mV}{4.5A} = 8.33m\Omega$$

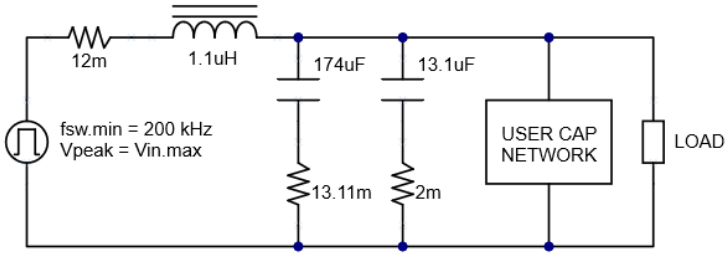
$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}} = \frac{8.33m\Omega * 13.11m\Omega}{13.11m\Omega - 8.33m\Omega} = 22.85m\Omega$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}} = \frac{50m\Omega}{22.85m\Omega} = 2.2 \rightarrow use\ 3\ output\ capacitors$$

$$C_{OUT-MAX} = \frac{10000\mu F}{V_{OUT}} = \frac{10000\mu F}{2.5} = 4000\mu F$$

In the example, 3x 330 µF/50 mΩ capacitors are needed. This is a total capacitance of 990 µF, which is well below the 4000 µF maximum allowed.

The output voltage ripple can be evaluated through simulation using the circuit below. This circuit incorporates worst-case conditions that include the effects of component tolerances, temperature extremes (-55 °C to 105 °C), and radiation (30 krad). Note that the resistor shown in series with the inductor includes the resistance of the inductor and power FETs. The pulsed voltage source should have a peak voltage equal to the input voltage and the minimum switching frequency (200 kHz) to evaluate the worst-case ripple. The duty cycle should be adjusted to attain the correct output voltage.




### 6.2.4 Choosing the Compensation Resistor and Capacitor Values

The VSCPL0510SG requires a series RC network to be placed across the +SENSE and TRIM pins. See Section 2.2 for a connection diagram. The required resistance and capacitance values depend on the amount of external capacitance ($C_x$) used and the ESR of those capacitors. If no external capacitor is used, then use the default compensation of $R_{comp}$ = 20 Ω and $C_{comp}$ = 2.7 nF. After selecting the type of capacitor to use for the external capacitance, calculate the frequency of the ESR zero. Use linear interpolation with the lookup tables below to calculate $R_{comp}$ and $C_{comp}$. Two capacitors in parallel can be used to get closer to the calculated value if necessary. It is recommended that only C0G or NP0 type capacitors be used for $C_{comp}$.

A lookup table showing values of $R_{comp}$ in Ohms is provided below.

| $C_x$ (µF) \ $f_{ESR}$ (kHz) | 7.2 | 20.7 | 120.5 |
|---|---|---|---|
| 0 | 20 | 20 | 20 |
| 220 | 20 | 20 | 20 |
| 880 | 700 | 300 | 20 |
| 2200 | 700 | 300 | 20 |
| 5060 | 700 | 300 | 20 |

A lookup table showing values of $C_{comp}$ in nF is provided below.

| $C_x$ (µF) \ $f_{ESR}$ (kHz) | 7.2 | 20.7 | 120.5 |
|---|---|---|---|
| 0 | 2.7 | 2.7 | 2.7 |
| 220 | 2.7 | 3.3 | 3.7 |
| 880 | 4.9 | 6.6 | 10.3 |
| 2200 | 11.5 | 15 | 20.2 |
| 5060 | 29.5 | 33 | 38.2 |

For example, suppose the total external capacitance was chosen to be 2.5 mF and composed of ten 250 µF in parallel, each with an ESR of 11.6 mΩ. The ESR frequency can be calculated as

$$f_{ESR} = \frac{1}{2\pi \times C \times ESR} = \frac{1}{2\pi \times 250\mu F \times 11.6m\Omega} = 55kHz.$$

Linear interpolation of the above lookup tables can be used to find an appropriate value for $C_{comp}$ and $R_{comp}$. First, interpolate across $C_x$ to find $C_{comp}$ at 20.7 kHz and at 120.5 kHz.

$$C_{comp}(C_x, f_{ESR}) = \frac{C_{comp_Cx0} \times (C_{x1} - C_x) + C_{comp_Cx1} \times (C_x - C_{x0})}{C_{x1} - C_{x0}}$$

$$C_{comp}(2.5mF, 20.7kHz) = \frac{15nF \times (5.06mF - 2.5mF) + 33nF \times (2.5mF - 2.2mF)}{5.06mF - 2.2mF} = 16.89nF$$

$$C_{comp}(2.5mF, 120.5kHz) = \frac{20.2nF \times (5.06mF - 2.5mF) + 38.2nF \times (2.5mF - 2.2mF)}{5.06mF - 2.2mF} = 22.09nF$$

Then interpolate across frequency using the previously calculated values.

$$C_{comp}(C_x, f_{ESR}) = \frac{C_{comp_f0} \times (f_1 - f_{ESR}) + C_{comp_f1} \times (f_{ESR} - f_0)}{f_1 - f_0}$$

$$C_{comp}(2.5mF, 55kHz) = \frac{16.89nF \times (120.5kHz - 55kHz) + 22.09nF \times (55kHz - 20.7kHz)}{120.5kHz - 20.7kHz} = 18.68nF$$

A standard 18 nF capacitor in parallel with a 0.68 nF capacitor can be chosen. A single 18 nF capacitor may also be chosen instead as $C_{comp}$ is not sensitive (within 5%) for values of external capacitance above 1mF.

Likewise, linear interpolation is used to calculate $R_{comp}$

$$R_{comp}(C_x, f_{ESR}) = \frac{R_{comp_f0} \times (f_1 - f_{ESR}) + R_{comp_f1} \times (f_{ESR} - f_0)}{f_1 - f_0}$$

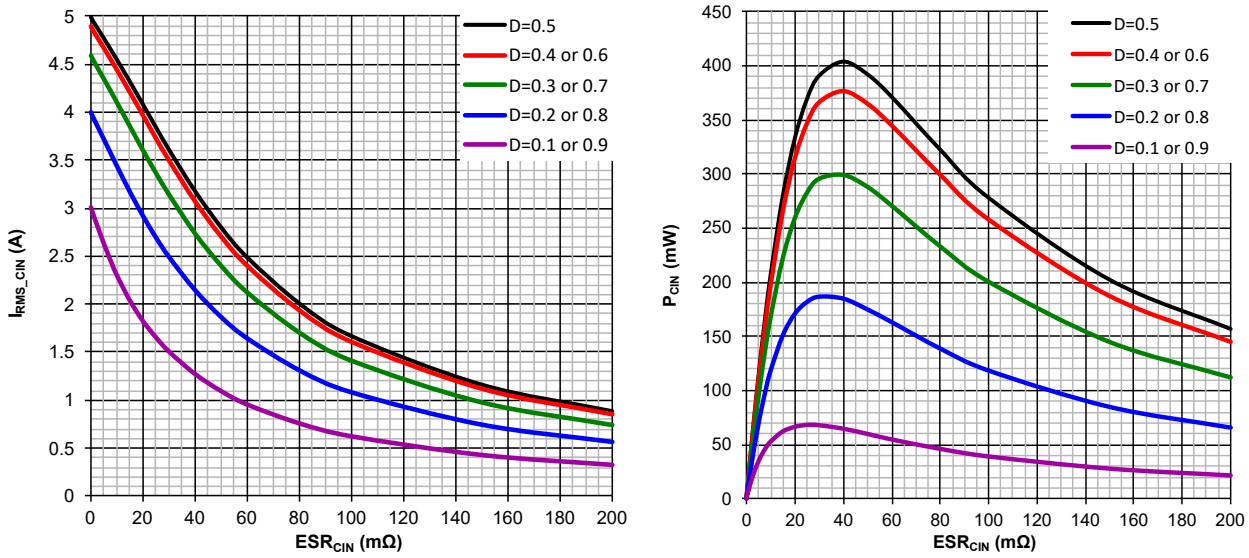
$$R_{comp}(2.5mF, 55kHz) = \frac{300\Omega \times (120.5kHz - 55kHz) + 20\Omega \times (55kHz - 20.7kHz)}{120.5kHz - 20.7kHz} = 203.77\Omega$$

A standard 200 Ω resistor is chosen as $R_{comp}$ is not sensitive (within 10%).

### 6.2.5 Input Capacitors

A minimum input capacitance of 100 µF should be added between VIN and GND to maintain the input voltage during transient conditions. The VSCPL0510SG has been designed with internal ceramic input capacitors to minimize the voltage stresses on its power MOSFETs. These ceramic capacitors also reduce the current stress in the user-added input capacitors. For 100 µF or greater capacitors, the RMS currents of the added capacitors will be determined primarily by their combined ESR. The curves below estimate the total RMS current in the added input capacitors for different $V_{OUT}/V_{IN}$ ratios. Worst-case conditions for load current, internal capacitance, and switching frequency are used. To verify that the capacitors will have sufficient margin, the RMS current ratings of the external capacitors can be compared to the appropriate curve. If the application $V_{OUT}/V_{IN}$ ratio is between two curves, interpolate between curves or use the curve with higher RMS current to be conservative. If multiple capacitors are added, then the RMS current will divide between them based on the equivalent ESR. If the maximum application load current is less than the VSCPL0510SG maximum of 10 A, then the RMS current will be reduced proportionally.

**Input Capacitor RMS Current and Power dissipation at 5V Input and 10A Output**




For example, let us assume Vin = 5 V, Vout = 1.8 V, max Iout = 5 A, and maximum temperature = 85 °C. Also, assume the capacitor being considered is a 150 µF capacitor with an ESR of 30 mΩ at 85 °C. Assume the capacitor's RMS current rating is 2.7 A at 85 °C. First, determine the Vout/Vin ratio:

$$D = \frac{V_{out}}{V_{in}} = \frac{1.8V}{5V} = 0.36$$

The ratio lies between the D = 0.3 and D = 0.4 curves. Use the D = 0.4 curve, as it has higher RMS current and gives a more conservative estimate. At 30 mΩ, the D = 0.4 curve indicates an RMS current of 3.5A. The RMS current for this application is found as:

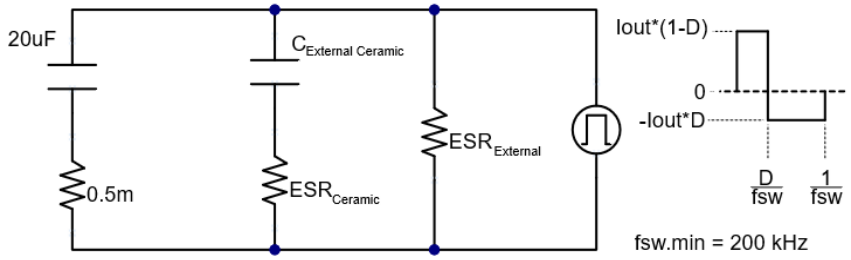
$$I_{RMS_CIN} = I_{RMS_CURVE}\left(\frac{Application\ \max I_{out}}{VSCPL\ \max I_{out}}\right) = 3.5A\left(\frac{5A}{10A}\right) = 1.75A$$

The RMS current in the added external input capacitor is 1.75 A, which is 65% of the 2.7 A current rating. The power dissipated in the capacitor will be about 42% of its power rating ($0.65^2 = 0.42$).

In another example, suppose Vin = 5 V, Vout = 1.25V, and max Iout = 10 A using the same capacitor as the previous example. Here, the Vout/Vin ratio is D = 0.25. Using the D = 0.3 curve, the RMS current is about 3.1 A, which exceeds the current rating of the added input capacitor. In this case, it will be necessary to use capacitors in parallel. Three capacitors in parallel gives an equivalent ESR of 10 mΩ. From the D = 0.3 curve, the total RMS current is 4.1 A. The RMS current of each capacitor is found as:

$$I_{RMS_CIN_PARALLEL} = \frac{I_{RMS_{CURVE}}}{N_{CAPACITORS}}\left(\frac{Application\ \max I_{out}}{VSCPL\ \max I_{out}}\right) = \frac{4.1A}{3}\left(\frac{10A}{10A}\right) = 1.4A$$

Alternatively, a simulation of the circuit below using a pulsed current source may be used to estimate the RMS current.




Here, an optional external large value ceramic capacitor (taking into account tolerance, temperature, and DC bias effects) may be added in parallel to reduce the RMS current flowing through the external tantalum capacitor.

## 6.3 PROTECTION FEATURES

### 6.3.1 Input Undervoltage Lockout

The VSCPL0510SG Series provides input undervoltage lockout protection with hysteresis. See Section 3.2, INPUT and OUTPUT STATIC, for details. For input voltages below the turn-on voltage, the converter will remain off. When the input voltage exceeds the turn-on voltage, the converter will start. For input voltages below the operating range of the converter but above the UVLO turn-off voltage, the converter may reach its maximum duty cycle, and the output may be out of regulation.

### 6.3.2 Output Soft Start

The VSCPL0510SG Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately 8 ms. The soft-start function is active whether the module is turned on with an application of input voltage or from release of the INH pin. The turn-on delay time is specified from the application of input voltage (or release of INH pin) until the output reaches 90% of its final value.

### 6.3.3 Output Short Circuit Protection

The VSCPL0510SG Series provides output short circuit protection. When a short circuit current is detected (approximately 20 A), the converter will shut down and enter a hiccup mode. After a delay, the converter will attempt a soft-start. This sequence will continue until the fault is removed, allowing the converter to soft-start and resume normal operation.

## 6.4 THERMAL CONSIDERATIONS

The VSCPL0510SG Series is rated for full power operation at 105 °C. Operation above 105 °C is allowed at reduced power. Specifically, the output power should be derated linearly from full power at 105 °C to half power at 110 °C and to zero power at 115 °C. The operating temperature of the converter is specified on the baseplate of the underside of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB or other thermal surface.

The DC-DC converter contains many semiconductor components. The maximum temperature rise from junction to case is 17 °C at full load.

## 6.5 RADIATION HARDNESS ASSURANCE

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's internal Space COTS Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for assuring the performance of VPT Space COTS products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, the converters were characterized for Enhanced Low Dose Rate Sensitivity (ELDRS) by testing samples at 10 - 100 mrad(Si)/s to 30 krad(Si). Radiation tolerance is assured by a combination of both module-level characterization and sample HDR TID testing of sequestered lots of all sensitive semiconductor piece-parts used within the module.

### 6.5.1 Radiation Test and Performance Levels

| Radiation Environment | | Module-Level Characterization |
|---|---|---|
| Total Ionizing Dose (TID) | High Dose Rate (HDR) | 30 krad(Si) |
| | Low Dose Rate (LDR) | 30 krad(Si) |
| Single-Event Effects (SEE) | Destructive (SEB, SEGR, SEL) | ≥ 42 MeV/mg/cm$^2$ |
| | Non-Destructive (SET, SEU, SEFI) | ≥ 30 MeV/mg/cm$^2$ |

### 6.5.2 RHA Plan Summary

| Test | RHA Plan for VSC Series DC-DC Converters |
|---|---|
| Total Ionizing Dose (TID): | Sensitive semiconductor components undergo RLAT to 40 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 30 krad(Si). |
| Enhanced Low Dose Rate Sensitivity (ELDRS): | Converters were tested at 10 - 100 mrad(Si)/s up to 30 krad(Si). |
| Single Event Effects (SEE): | Converters are characterized to LET ≥ 42 MeV/mg/cm$^2$ for catastrophic events (SEL, SEB, SEGR) and to LET ≥ 30 MeV/mg/cm$^2$ for transients (SET) and functional interrupts (SEFI) under heavy ion exposure. |
| Radiation Lot Acceptance Testing (RLAT): | All production lots of sensitive semiconductor components undergo a sample test for TID at HDR or LDR. |

## 7.0 ENVIRONMENTAL SCREENING

| Test | /ES+ |
|---|---|
| Internal Visual | IPC-A-610, Class 3 |
| Temperature Cycling | MIL-STD-883, Method 1010, Condition B, -55 °C to +125 °C, 10 Cycles |
| Burn In | 96 hours at +105 °C |
| Final Electrical | -55 °C, 25 °C, 105 °C[1] |
| External Visual | Internal Procedure |

1. 100% R&R testing with all test data included in product shipment

## 8.0 ORDERING INFORMATION

| VSCPL | 05 | 10 | S | G | /ES+ |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

| (1) Product Series | (2) Nominal Input Voltage | (3) Output Current | (4) Number of Outputs | (5) Package Option | (6) Screening Code |
|---|---|---|---|---|---|
| **VSCPL** | **05** 5 Volts | **10** 10 Amps | **S** Single | **G** Gullwing | /ES+ |

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, and source inspection.

## 9.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

**Phone**: (425) 353-3010
**Fax**: (425) 353-4030
**E-mail**: vptsales@vptpower.com

All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

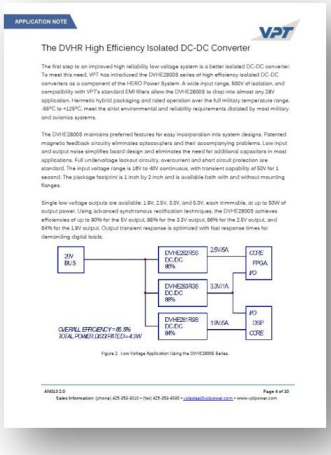
## 10.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

**Product Catalogs**




**Application Notes and White Papers**

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