



# VSCPL1210SG SERIES

## RADIATION TOLERANT DC-DC CONVERTERS



VSCPL1210SG - Exact marking may differ from that shown

### Models Available

Input Range: 4.5 V to 13.2 V

Output Range: 0.6 V to 5 V, 10A

Wattage: up to 50 W

### 1.0 DESCRIPTION

The VSCPL1210SG Series is a commercial off the shelf DC-DC converter designed for the 'NewSpace' market. Performance is guaranteed through the use of radiation lot acceptance tested (RLAT) components. Our proprietary packaging creates a dual side heatsinking option with very low outgassing. The surface mount design enables streamlined reflow soldering alongside other SMT components for simplified board-level integration.

Radiation tested to 42 MeV/mg/cm<sup>2</sup> with no destructive SEE events (SEGR, SEB, and SEL) and tested to 40 krad(Si), guaranteed to 30 krad(Si), for TID in accordance with VPT's inhouse radiation hardness assurance (RHA) plan.

The VSCPL1210SG Series is designed for smaller satellites in low earth orbits (LEO), and NASA Class D missions where the balance of cost and guaranteed performance is critical.

### 1.1 FEATURES

- Operates from 4.5 – 13.2 V input
- Adjustable Output from 0.6 – 5 V
- Up to 10 Amps Output
- Peak efficiency up to 95%
- Output Inhibit Control
- Low Output Noise
- Short Circuit Protection
- Synchronizable to an external clock
- Continuous operation over the full temperature range of -55 °C to +105 °C with no power derating
- Surface-mount design for simplified production.

### 1.2 SPACE LEVEL CHARACTERIZATIONS

- Guaranteed TID performance to 30 krad(Si) including LDR
- SEE tested to 42 MeV/mg/cm<sup>2</sup>. Transients are fully analyzed for cross-section and magnitude at 30 MeV/mg/cm<sup>2</sup>
- Radiation Hardness Assurance, see Section 6.5 herein
- Mean Time Between Failures (MTBF) calculations available
- Failure In Time (FIT) numbers available

### 1.3 MANUFACTURING AND COMPLIANCE

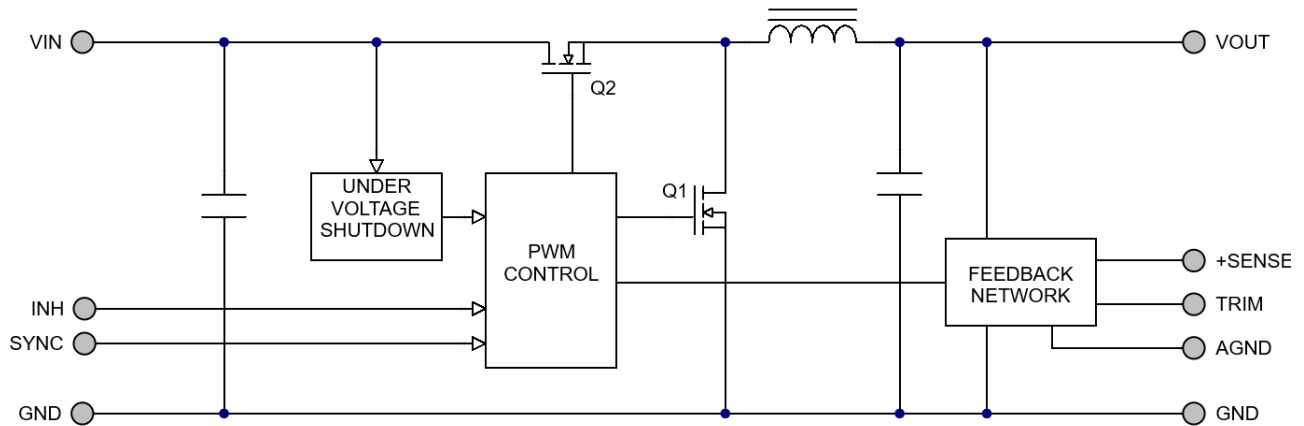
- Manufactured in an ISO9001, J-STD-001, and IPC-A-610 certified facility.

### 1.4 PACKAGING

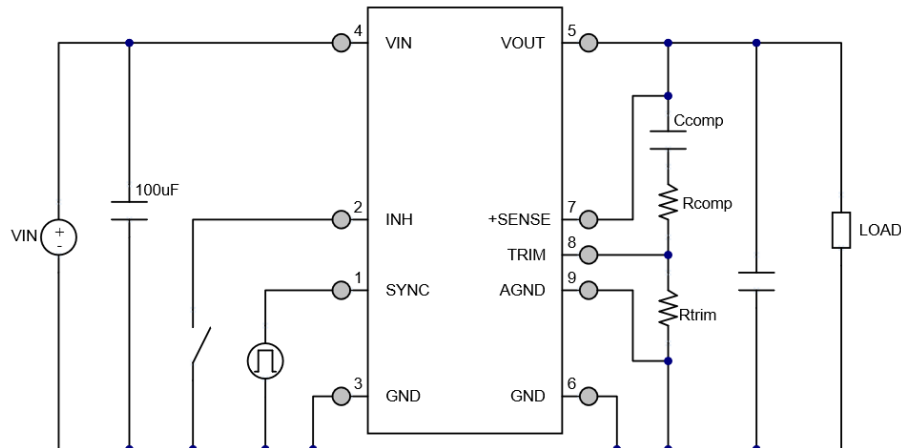
- Low-profile: 1.2" x 1.2" x 0.40"
- Max weight: 32 g

## 2.0 DIAGRAMS

### 2.1 BLOCK DIAGRAM



### 2.2 CONNECTION DIAGRAM



1. Rtrim should be connected directly across pins 8 and 9 as close as possible to the VSCPL.
2. AGND should be connected to GND close to the VSCPL. Voltage difference between the AGND and the GND pins greater than 0.3 V may result in regulation error and/or damage to the VSCPL.
3. If not using INH, leave pin 2 open.
4. If not using SYNC, leave pin 1 open or connected to GND.
5. Rcomp and Ccomp form part of the converter's compensation network. See Section 6.2.4 for guidelines on selecting values.

## 3.0 SPECIFICATIONS

### 3.1 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings			
Input Voltage (Continuous):	-0.5 V to 13.2 V	Operating Temperature (Full Load):	-55 °C to +105 °C
Input Voltage (Transient, 1 second):	-0.5 V to 14 V	Storage Temperature:	-55 °C to +125 °C
AGND	-0.3 V to 0.3 V	Lead Solder Temperature (10 seconds):	300 °C

## 3.2 PERFORMANCE SPECIFICATIONS

Tcase = -55 °C to +105 °C, Vin = +5 V ± 5% or +12V ± 5%, Full Load, Unless Otherwise Specified

Parameter	Conditions <sup>1</sup>	VSCPL1210SG			Units
		Min	Typ	Max	
<b>INPUT</b>					
Voltage <sup>2</sup>	Continuous	4.5	-	13.2	V
Current	INH = GND	-	35	50	mA
	Vin = 5 V, Vout = 3.3V, No Load	-	65	150	mA
	Vin = 12 V, Vout = 5V, No Load	-	100	180	mA
Undervoltage Lockout <sup>2,3</sup>	Turn-On	4	4.3	4.45	V
	Turn-Off	3.3	3.5	3.8	V
<b>OUTPUT STATIC</b>					
Voltage	Tcase = 25 °C	-1.0	-	+1.0	%Vout
	Tcase = -55 °C to +105 °C	-1.5	-	+1.5	%Vout
Power <sup>4</sup>		0	-	50	W
Current	Continuous	0	-	10	A
Ripple Voltage	Vin = 5 V, Vout = 3.3 V, 20 Hz to 10 MHz	-	25	60	mVpp
	Vin = 12 V, Vout = 5 V, 20 Hz to 10 MHz	-	50	120	mVpp
Load Regulation	No Load to Full Load	-	0	0.2	%
Short Circuit Power Dissipation	Vin = 12V, Vout = 5V prior to short circuit	-	0.7	2	W
<b>OUTPUT DYNAMIC</b>					
Load Step, Half to Full Load, Vin = 5 V, Vout = 3.3 V	Output Transient	-	80	120	mVpk
	Recovery <sup>5</sup>	-	30	100	µs
Turn-On, Vin = 0 V to 5 V or 12 V	Delay	-	8	10	ms
	Overshoot	-	0	15	mVpk
<b>FUNCTION</b>					
INH Pin Input <sup>2</sup>	Output Inhibited	0	-	0.3	V
INH Pin Open Circuit Voltage <sup>2</sup>	Output Enabled	-	3.8	5	V
SYNC Frequency Range	V <sub>H</sub> - V <sub>L</sub> = 5 V, D = 20-80%	250	-	300	kHz
<b>GENERAL</b>					
Efficiency, Full Load	Vin = 5 V, Vout = 3.3V	90	94	-	%
Capacitive Load <sup>2</sup>	Vout ≤ 2 V	-	-	5000	µF
	Vout ≥ 2 V	-	-	$\frac{10000}{Vout}$	µF
Switching Frequency		200	250	300	kHz
Weight		-	-	32	g
MTBF (MIL-HDBK-217F)	SF @ Tcase = 55 °C	-	22.5	-	MHr
<b>POST-RAD LIMITS<sup>6</sup></b>					
Output Voltage	Tcase = -55 °C to +105 °C	-2.0	-	+2.0	%Vout

1. Performance specifications are guaranteed with 100 µF from VIN to GND.

2. Verified by initial electrical design verification. Post design verification, parameter shall be guaranteed to the limits specified.

3. Output voltage not necessarily in regulation.

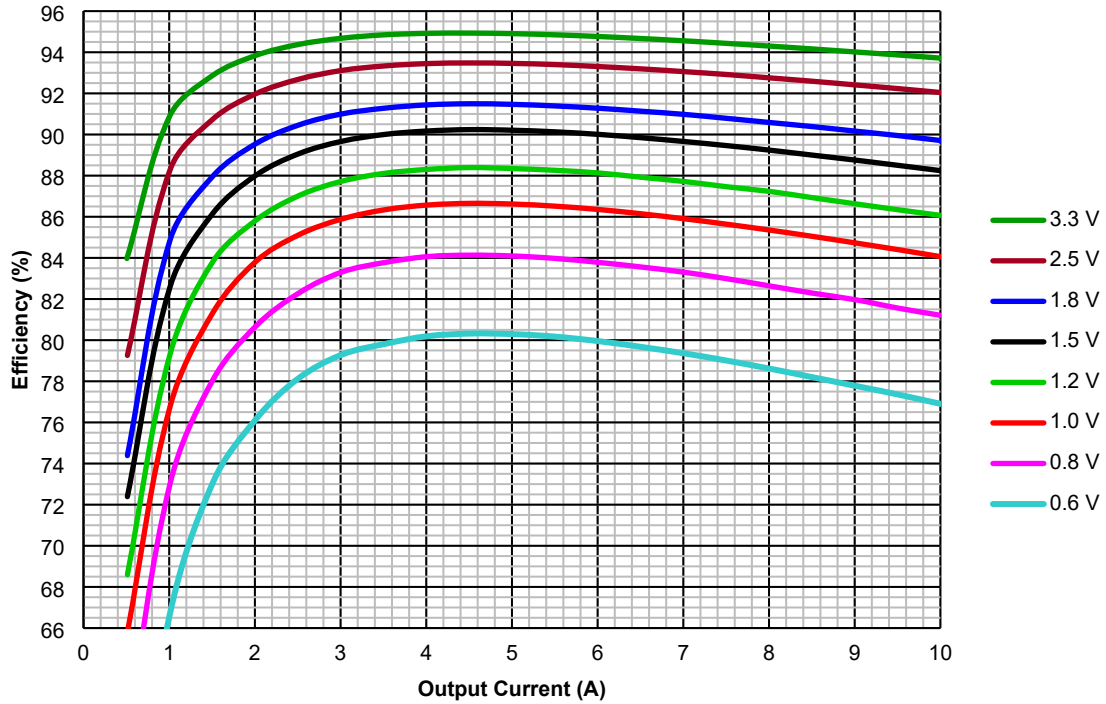
4. Dependent on output voltage.

5. Time for output voltage to settle within 1% of steady-state value.

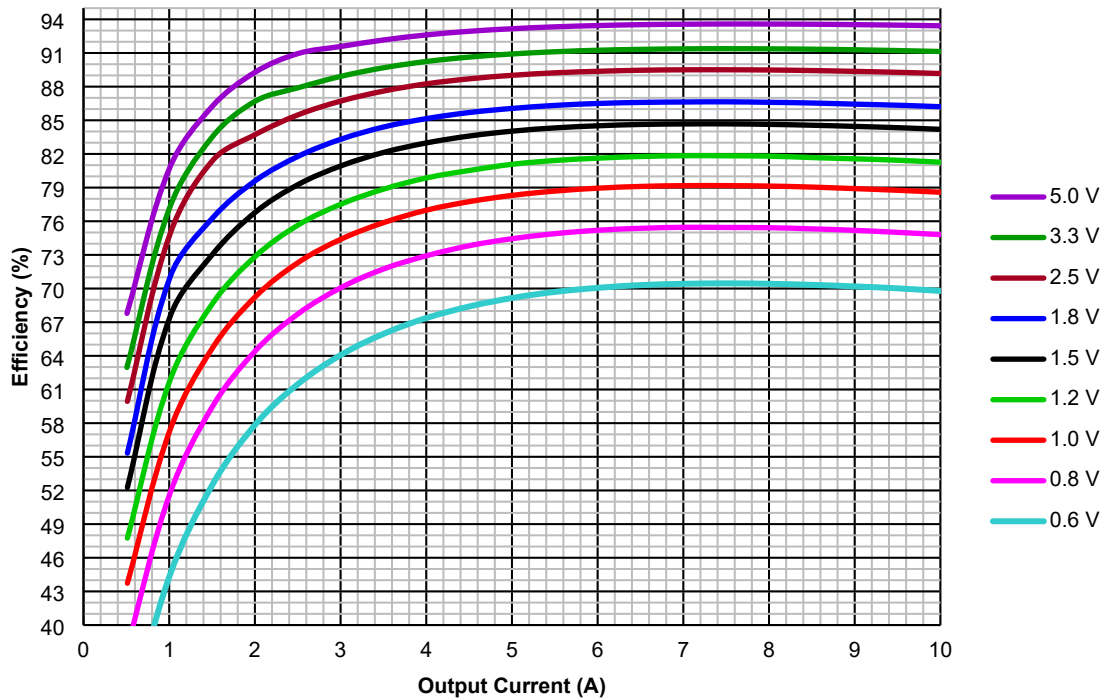
6. Post-RAD limits are within standard limits except where noted.

## 4.0 PERFORMANCE CURVES

### 4.1.1 VSCPL1210SG Efficiency (Typical, 25 °C, Vin=5V)

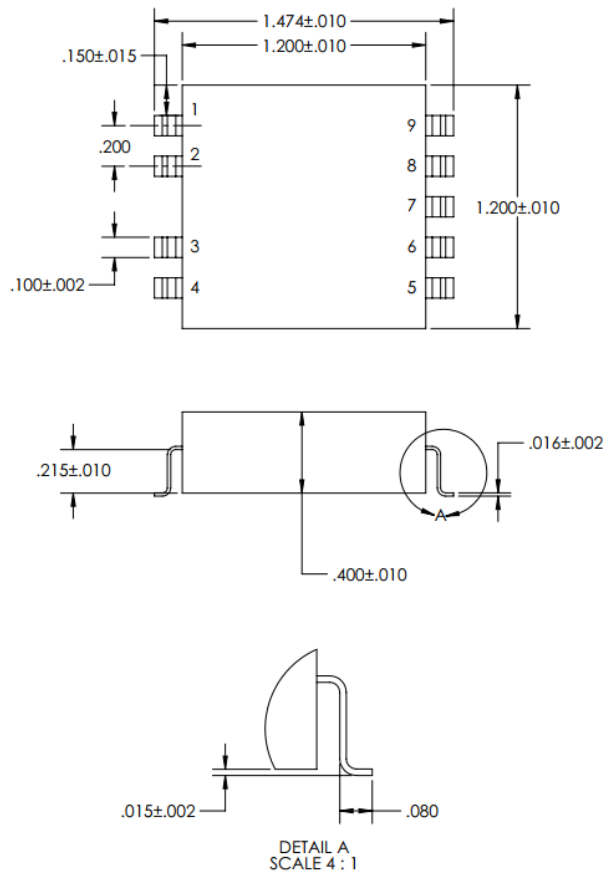


### 4.1.2 VSCPL1210SG Efficiency (Typical, 25 °C, Vin=12V)



## 5.0 MECHANICAL OUTLINES AND PINOUT

Standard Package Option:



1. Tolerances are  $\pm 0.010$ " unless otherwise stated.
2. Case temperature is measured on the center of the baseplate surface on the underside of the converter.
3. Materials: Body (Epoxy); Pin (Copper, alloy 110, gold over nickel plating).

Pin	Function	Pin	Function
1	SYNC	5	VOUT
2	INHIBIT	6	GND
3	GND	7	+SENSE
4	VIN	8	TRIM
		9	AGND

## 6.0 TECHNICAL NOTES

Please note that many of these functions are also demonstrated in detail on the VPT website in the form of technical video labs.

### 6.1 GENERAL INFORMATION

#### 6.1.1 Topology Description

The VSCPL1210SG is a non-isolated, fixed-frequency, radiation-tolerant, synchronous buck converter. It operates from a 4.5 V to 13.2 V input range and provides a stepped-down, precisely regulated, programmable output voltage at high efficiency. The VSCPL1210SG is optimized for low voltage point-of-load (POL) applications.

#### 6.1.2 External Components

The VSCPL1210SG Series has internal input and output capacitors. To meet the performance specifications in Section 3.2, a minimum additional 100  $\mu\text{F}$  tantalum input decoupling capacitor is required. The VSCPL1210SG is stable with no load capacitance. Additional output capacitance is allowed up to the maximum listed in Section 3.2. An external resistor across the TRIM and AGND pins set the output voltage. The output voltage defaults to 0.6 V if no resistor is used. A series RC network must be placed across the +SENSE and TRIM pins in order to provide compensation to the converter's control loop. Section 6.2.4 gives guidelines for selecting values.

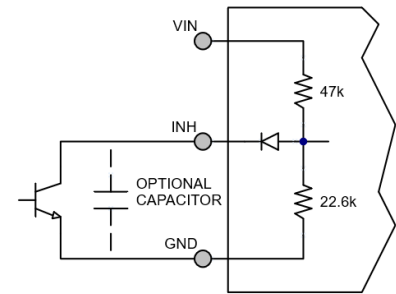
#### 6.1.3 Source Impedance

The impedance of the input source can interact with the POL converter and impact performance. High source impedance is often caused by a long input cable or other components added in series with the input. In some cases, additional input capacitance will be needed to stabilize the system.

### 6.2 FUNCTION DESCRIPTIONS

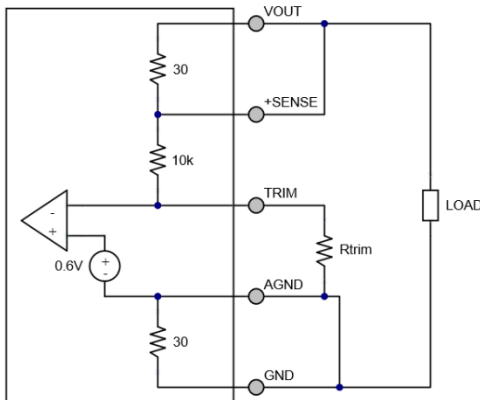
#### 6.2.1 On/Off Control (Inhibit)

The INH (Inhibit) pin is a control pin referenced to GND. The INH pin must be driven using an open collector or open drain configuration. Pulling the INH pin low disables the converter output. Leaving INH open enables the output, allowing the converter to operate normally. The pin must be pulled below 0.3 V to disable the output. An optional capacitor from INH to GND may be used to delay turn-on. The INH pin should be left open if not used.



#### 6.2.2 Adjusting the Output Voltage (TRIM)

The output voltage of the converter is set with an external resistor connected from the TRIM pin to the AGND pin. Use the equations or table below to choose the trim resistor value. Choose the next closest standard resistor value. Greater precision for non-standard Trim resistor values can be obtained using a parallel combination of standard resistors. A trim resistor tolerance of 0.1% is recommended to achieve an accurate output voltage. The default output voltage with the TRIM pin left open is 0.6 V.



$$R_{TRIM} = \frac{6000\Omega}{V_{OUT} - 0.6V}$$

$$V_{OUT} = \frac{6000\Omega}{R_{TRIM}} + 0.6V$$

VSCPL1210SG		
+Vout (V)	Rtrim ( $\Omega$ )	Parallel Combination ( $\Omega$ )
0.6	Open	-
0.8	30k	-
0.9	20k	-
1.0	15k	-
1.2	10k	-
1.5	6.6667k	10k    20k -or- 12k    15k
1.8	5k	10k    10k -or- 7.5k    15k
2.0	4.2857k	7.5k    10k
2.5	3.1579k	3.16k    4750k
2.8	2.7273k	3k    30k -or- 2.8k    105k
3.0	2.5k	3k    15k
3.3	2.2222k	2.4k    30k
3.4	2.14289k	2.4k    20k
3.6	2k	-
3.7	1.9355k	2.4k    10k
4.0	1.7647k	2k    15k
5.0	1.3636k	1.5k    15k

## 6.2.3 Output Capacitors

Output capacitors for point-of-load (POL) DC/DC converters should be chosen to meet output voltage ripple and transient requirements. Meeting the transient response requirement is accomplished by making the output impedance of the converter sufficiently small. Given the high control bandwidth of POL converters like the VSCPL series, the peak output impedance is typically dominated by the equivalent series resistance (ESR) of the bulk output capacitance. Therefore, the output capacitors should be chosen to set a certain maximum total ESR. The total ESR is the parallel combination of the internal bulk capacitor's ESR and that of the added capacitors. Given the output voltage transient requirement, maximum load step, and the ESR of each bulk capacitor that will be added, the number of added capacitors needed is calculated with the following equations:

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}}$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}}$$

Parameter	Definition
$\Delta V_{OUT}$	Max $V_{OUT}$ transient allowed
$\Delta I_{OUT}$	Max load current step
$ESR_{TOTAL}$	Total combined parallel ESR, including internal and added capacitors
$ESR_{ADDED}$	Combined parallel ESR of the added capacitors
$ESR_{INTERNAL}$	ESR of the internal bulk capacitor <b>(13.11 mΩ max under worst-case conditions)</b>
$ESR_{EACH}$	ESR of each of the added capacitors
N	Number of added capacitors

Make sure that the added capacitance does not violate the maximum allowed output capacitance using the following equation (up to 5000μF):

$$C_{OUT-MAX} = \frac{10000\mu F}{V_{OUT}}$$

For example, assume that  $V_{OUT}$  is 2.5 V, the maximum output transient allowed is 37.5mV, and the load step is 4.5 A. Assume the output capacitors being used are 330 μF and have a maximum ESR of 50 mΩ each.

$$ESR_{TOTAL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{37.5mV}{4.5A} = 8.33m\Omega$$

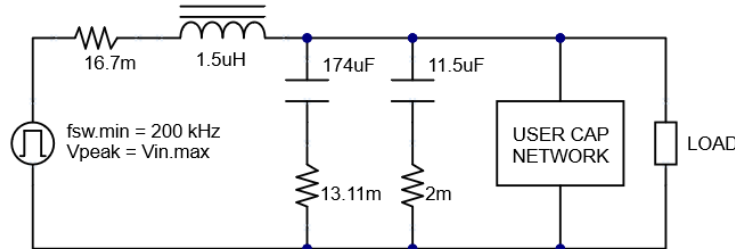
$$ESR_{ADDED} = \frac{ESR_{TOTAL} * ESR_{INTERNAL}}{ESR_{INTERNAL} - ESR_{TOTAL}} = \frac{8.33m\Omega * 13.11m\Omega}{13.11m\Omega - 8.33m\Omega} = 22.85m\Omega$$

$$N = \frac{ESR_{EACH}}{ESR_{ADDED}} = \frac{50m\Omega}{22.85m\Omega} = 2.2 \rightarrow \text{use 3 output capacitors}$$

$$C_{OUT-MAX} = \frac{10000\mu F}{V_{OUT}} = \frac{10000\mu F}{2.5} = 4000\mu F$$

In the example, 3x 330 μF/50 mΩ capacitors are needed. This is a total capacitance of 990 μF, which is well below the 4000 μF maximum allowed.

The output voltage ripple can be evaluated through simulation using the circuit below. This circuit incorporates worst-case conditions that include the effects of component tolerances, temperature extremes (-55 °C to 105 °C), and radiation (30 krad). Note that the resistor shown in series with the inductor includes the resistance of the inductor and power FETs. The pulsed voltage source should have a peak voltage equal to the input voltage and the minimum switching frequency (200 kHz) to evaluate the worst-case ripple. The duty cycle should be adjusted to attain the correct output voltage.



### 6.2.4 Choosing the Compensation Resistor and Capacitor Values

The VSCPL1210SG requires a series RC network to be placed across the +SENSE and TRIM pins. See Section 2.2 for a connection diagram. The required resistance and capacitance values depend on the amount of external capacitance ( $C_x$ ) used and the ESR of those capacitors. If no external capacitor is used, then use the default compensation of  $R_{comp} = 20 \Omega$  and  $C_{comp} = 2.7 \text{ nF}$ . After selecting the type of capacitor to use for the external capacitance, calculate the frequency of the ESR zero. Use the equations in the table below or the lookup table to calculate  $C_{comp}$ . Choose the next closest standard value. Two capacitors in parallel can be used to get closer to the calculated value if desired. It is recommended that only COG or NP0 type capacitors be used for  $C_{comp}$ .

Use  $R_{comp} = 20 \Omega$  when  $f_{ESR} \geq 20 \text{ kHz}$  and the equation below for  $f_{ESR} < 20 \text{ kHz}$ .

$$R_{comp}[\Omega] = 20\Omega, \quad f_{ESR} \geq 20\text{kHz}$$

$$R_{comp}[\Omega] = -13.33f_{ESR}[\text{kHz}] + 296, \quad f_{ESR} < 20\text{kHz}$$

$f_{ESR}$	$C_{comp}$	$R_{comp}$
220 $\mu\text{F}$ , 100 $\text{m}\Omega$ 7.2 kHz	$C_{comp}[\text{nF}] = 0.0913C_x^2 + 0.28C_x + 2.7$	200 $\Omega$
220 $\mu\text{F}$ , 35 $\text{m}\Omega$ 20.7 kHz	$C_{comp}[\text{nF}] = -0.059C_x^2 + 1.53C_x + 2.7$	20 $\Omega$
220 $\mu\text{F}$ , 6 $\text{m}\Omega$ 120.5 kHz	$C_{comp}[\text{nF}] = -0.209C_x^2 + 3.39C_x + 2.7$	20 $\Omega$

$C_x$  = Total external capacitance in  $\text{mF}$

A lookup table showing interpolated values of  $C_{comp}$  in  $\text{nF}$  is provided below.

$C_x$ (mF) \ $f_{ESR}$ (kHz)	7.2	10	15	20.7	30	50	70	80	100	120.5
0.0	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7
0.5	2.9	3.0	3.3	3.5	3.6	3.9	4.1	4.1	4.2	4.3
1.0	3.1	3.4	3.8	4.2	4.5	5.0	5.3	5.5	5.7	5.9
1.5	3.3	3.8	4.4	4.9	5.4	6.1	6.5	6.7	7.0	7.3
2.0	3.6	4.2	5.0	5.5	6.2	7.1	7.7	7.9	8.3	8.6
2.5	4.0	4.7	5.5	6.2	7.0	8.0	8.7	9.0	9.5	9.9
3.0	4.4	5.2	6.1	6.8	7.7	8.9	9.7	10.0	10.5	11.0
3.5	4.8	5.6	6.7	7.3	8.4	9.7	10.5	10.9	11.4	12.0
4.0	5.3	6.2	7.2	7.9	9.1	10.5	11.4	11.7	12.3	12.9
4.5	5.8	6.7	7.8	8.4	9.7	11.2	12.1	12.5	13.1	13.7
5.0	6.4	7.2	8.4	8.9	10.2	11.7	12.7	13.0	13.7	14.4

Example 1: The external capacitance is selected to be 0.88 mF, composed of four 220µF 35mOhm capacitors in parallel. The frequency of the ESR zero is then

$$f_{ESR} = \frac{1}{2\pi \times C \times ESR} = \frac{1}{2\pi \times 220\mu F \times 35m\Omega} = 20.7kHz.$$

From the equation in the table,

$$C_{comp}[nF] = -0.059(0.88)^2 + 1.53 \times 0.88 + 2.7 = 4nF$$

$R_{comp}$  is 20 Ω since  $f_{ESR}$  is greater than 20 kHz, and a single 3.9 nF capacitor is chosen for  $C_{comp}$ .

Example 2: Suppose the total external capacitance was chosen to be 2.2 mF and the frequency of the ESR zero was 55 kHz. Linear interpolation of the lookup table can be used to find an appropriate value for  $C_{comp}$ . First, interpolate across  $C_x$  to find  $C_{comp}$  at 50 kHz and at 70 kHz.

$$C_{comp}(C_x, f_{ESR}) = \frac{C_{comp_{Cx0}} \times (C_{x1} - C_x) + C_{comp_{Cx1}} \times (C_x - C_{x0})}{C_{x1} - C_{x0}}$$

$$C_{comp}(2.2mF, 50kHz) = \frac{7.1nF \times (2.5mF - 2.2mF) + 8nF \times (2.2mF - 2.0mF)}{2.5mF - 2.0mF} = 7.46nF$$

$$C_{comp}(2.2mF, 70kHz) = \frac{7.7nF \times (2.5mF - 2.2mF) + 8.7nF \times (2.2mF - 2.0mF)}{2.5mF - 2.0mF} = 8.1nF$$

Then interpolate across frequency using the previously calculated values.

$$C_{comp}(C_x, f_{ESR}) = \frac{C_{comp_{f0}} \times (f_1 - f_{ESR}) + C_{comp_{f1}} \times (f_{ESR} - f_0)}{f_1 - f_0}$$

$$C_{comp}(2.2mF, 55kHz) = \frac{7.46nF \times (70kHz - 55kHz) + 8.1nF \times (55kHz - 50kHz)}{70kHz - 50kHz} = 7.62nF$$

A standard 6.8 nF capacitor in parallel with a 0.82 nF capacitor can be chosen.

Example 3: Suppose  $f_{ESR} = 15$  kHz with  $C_x = 3$  mF.  $C_{comp}$  is 6.1 nF from the lookup table, and  $R_{comp}$  can be found by linear interpolation such that

$$R_{comp}[\Omega] = -13.33f_{ESR}[kHz] + 296, f_{ESR} < 20kHz$$

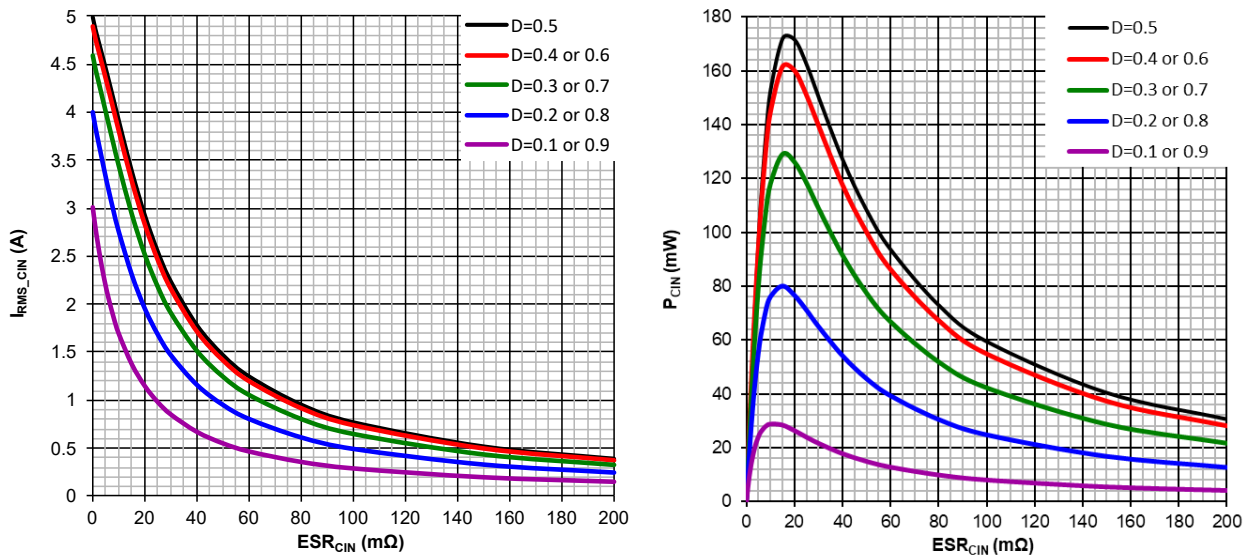
$$R_{comp}[\Omega] = -13.33 \times 15kHz + 296 = 96\Omega$$

A standard value for  $R_{comp}$  can be chosen to be 100 Ω as its value is not sensitive.

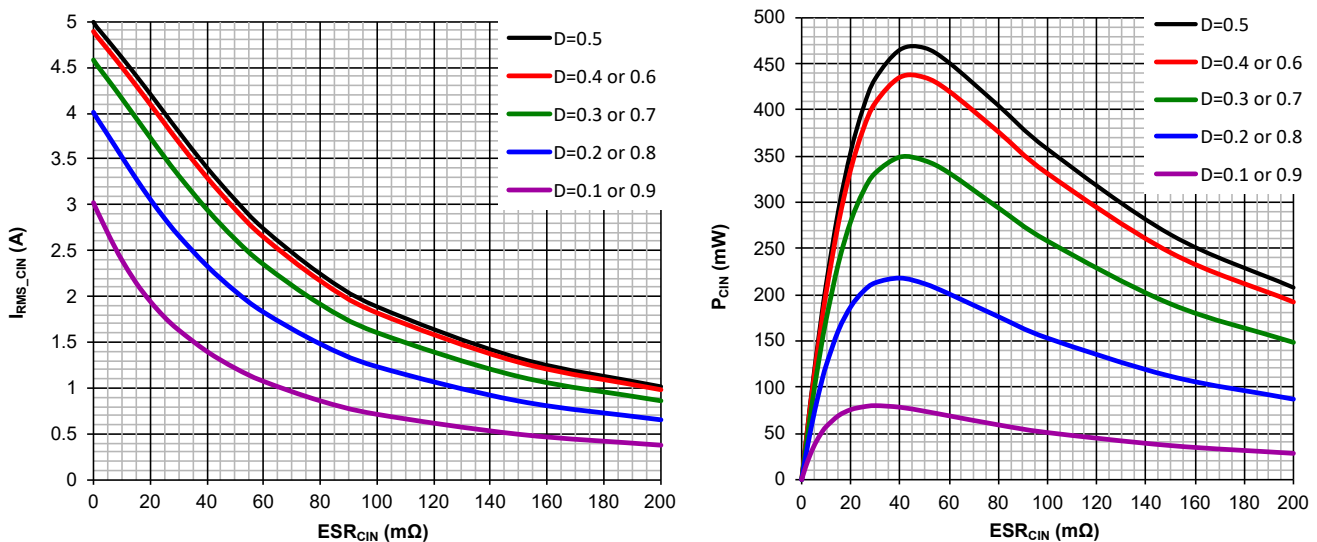
## 6.2.5 Input Capacitors

A minimum input capacitance of 100  $\mu\text{F}$  should be added between  $V_{\text{IN}}$  and GND to maintain the input voltage during transient conditions. The VSCPL1210SG has been designed with internal ceramic input capacitors to minimize the voltage stresses on its power MOSFETs. These ceramic capacitors also reduce the current stress in the user-added input capacitors. For 100  $\mu\text{F}$  or greater capacitors, the RMS currents of the added capacitors will be determined primarily by their combined ESR. The curves below estimate the total RMS current in the added input capacitors for different  $V_{\text{OUT}}/V_{\text{IN}}$  ratios. Worst-case conditions for load current, internal capacitance, and switching frequency are used. A set of curves is given for both 5V input voltage and 12V input voltage. The difference is due to the effect of DC bias on the capacitance of the internal ceramic capacitors. To verify that the capacitors will have sufficient margin, the RMS current ratings of the external capacitors can be compared to the appropriate curve. If the application  $V_{\text{OUT}}/V_{\text{IN}}$  ratio is between two curves, interpolate between curves or use the curve with higher RMS current to be conservative. If multiple capacitors are added, then the RMS current will divide between them based on the equivalent ESR. If the maximum application load current is less than the VSCPL1210SG maximum of 10 A, then the RMS current will be reduced proportionally.

**Input Capacitor RMS Current and Power dissipation at 5V Input and 10A Output**



**Input Capacitor RMS Current and Power dissipation at 12V Input and 10A Output**



For example, let us assume  $V_{in} = 5\text{ V}$ ,  $V_{out} = 1.8\text{ V}$ ,  $\text{max } I_{out} = 5\text{ A}$ , and maximum temperature =  $85\text{ }^\circ\text{C}$ . Also, assume the capacitor being considered is a  $150\text{ }\mu\text{F}$  capacitor with an ESR of  $30\text{ m}\Omega$  at  $85\text{ }^\circ\text{C}$  and the worst-case minimum switching frequency of  $200\text{ kHz}$ . Assume the capacitor's RMS current rating is  $2.7\text{ A}$  at  $85\text{ }^\circ\text{C}$ . First, determine the  $V_{out}/V_{in}$  ratio:

$$D = \frac{V_{out}}{V_{in}} = \frac{1.8\text{V}}{5\text{V}} = 0.36$$

The ratio lies between the  $D = 0.3$  and  $D = 0.4$  curves. Use the  $D = 0.4$  curve, as it has higher RMS current and gives a more conservative estimate. At  $30\text{ m}\Omega$ , the  $D = 0.4$  curve indicates an RMS current of  $2.2\text{ A}$ . The RMS current for this application is found as:

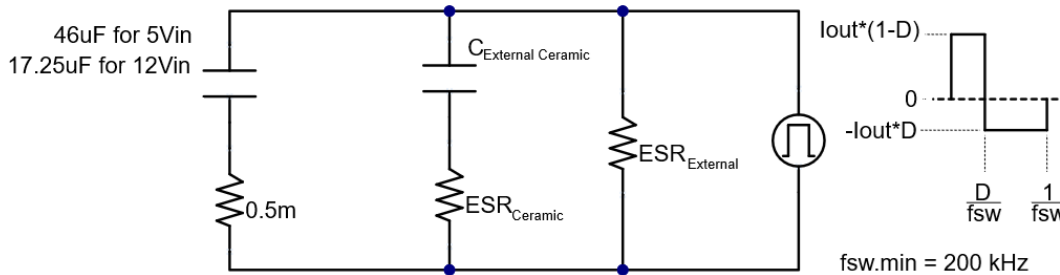
$$I_{RMS\_CIN} = I_{RMS\_CURVE} \left( \frac{\text{Application max } I_{out}}{VSCPL \text{ max } I_{out}} \right) = 2.2\text{A} \left( \frac{5\text{A}}{10\text{A}} \right) = 1.1\text{A}$$

The RMS current in the added external input capacitor is  $1.1\text{ A}$ , which is  $41\%$  of the  $2.7\text{ A}$  current rating. The power dissipated in the capacitor will be about  $17\%$  of its power rating ( $0.41^2 = 0.17$ ).

In another example, suppose  $V_{in} = 12\text{ V}$ ,  $V_{out} = 3\text{V}$ , and  $\text{max } I_{out} = 10\text{ A}$  using the same capacitor as the previous example. Here, the  $V_{out}/V_{in}$  ratio is  $D = 0.25$ . Using the  $D = 0.3$  curve, the RMS current is about  $3.3\text{ A}$ , which exceeds the current rating of the added input capacitor. In this case, it will be necessary to use capacitors in parallel. Three capacitors in parallel gives an equivalent ESR of  $10\text{ m}\Omega$ . From the  $D = 0.3$  curve, the total RMS current is  $4.2\text{ A}$ . The RMS current of each capacitor is found as:

$$I_{RMS\_CIN\_PARALLEL} = \frac{I_{RMS\_CURVE}}{N_{CAPACITORS}} \left( \frac{\text{Application max } I_{out}}{VSCPL \text{ max } I_{out}} \right) = \frac{4.2\text{A}}{3} \left( \frac{10\text{A}}{10\text{A}} \right) = 1.4\text{A}$$

Alternatively, a simulation of the circuit below using a pulsed current source may be used to estimate the RMS current.



Here, an optional external large value ceramic capacitor (taking into account tolerance, temperature, and DC bias effects) may be added in parallel to reduce the RMS current flowing through the external tantalum capacitor.

## 6.3 PROTECTION FEATURES

### 6.3.1 Input Undervoltage Lockout

The VSCPL1210SG Series provides input undervoltage lockout protection with hysteresis. See Section 3.2, INPUT and OUTPUT STATIC, for details. For input voltages below the turn-on voltage, the converter will remain off. When the input voltage exceeds the turn-on voltage, the converter will start. For input voltages below the operating range of the converter but above the UVLO turn-off voltage, the converter may reach its maximum duty cycle, and the output may be out of regulation.

### 6.3.2 Output Soft Start

The VSCPL1210SG Series utilizes an output soft-start function to ramp the output in a controlled manner, eliminating output voltage overshoot and limiting inrush current at turn on. A voltage mode soft-start ensures the output waveform remains consistent regardless of changes in the load current. The output rise time is approximately  $6\text{ ms}$ . The soft-start function is active whether the module is turned on with an application of input voltage or from release of the INH pin. The turn-on delay time is specified from the application of input voltage (or release of INH pin) until the output reaches  $90\%$  of its final value.

### 6.3.3 Output Short Circuit Protection

The VSCPL1210SG Series provides output short circuit protection. When a short circuit current is detected (approximately 25 A), the converter will shut down and enter a hiccup mode. After a delay, the converter will attempt a soft-start. This sequence will continue until the fault is removed, allowing the converter to soft-start and resume normal operation.

## 6.4 THERMAL CONSIDERATIONS

The VSCPL1210SG Series is rated for full power operation at 105 °C. Operation above 105 °C is allowed at reduced power. Specifically, the output power should be derated linearly from full power at 105 °C to half power at 110 °C and to zero power at 115 °C. The operating temperature of the converter is specified on the baseplate of the underside of the converter. The converter is designed to be conduction-cooled, with the baseplate mounted to a heat sink, chassis, PCB or other thermal surface.

The DC-DC converter contains many semiconductor components. The maximum temperature rise from junction to case is 26 °C at full load.

## 6.5 RADIATION HARDNESS ASSURANCE

VPT takes a conservative approach to radiation testing to ensure product performance in a space environment. VPT's internal Space COTS Radiation Hardness Assurance (RHA) plan documents VPT's processes and procedures for assuring the performance of VPT Space COTS products under various environmental conditions in space including Total Ionizing Dose (TID) and Single-Event Effects (SEE). Additionally, the converters were characterized for Enhanced Low Dose Rate Sensitivity (ELDRS) by testing samples at 10 - 100 mrad(Si)/s to 40 krad(Si). Radiation tolerance is assured by a combination of both module-level characterization and sample HDR TID testing of sequestered lots of all sensitive semiconductor piece-parts used within the module.

### 6.5.1 Radiation Test and Performance Levels

Radiation Environment		Piece Part RLAT	Module-Level Characterization
Total Ionizing Dose (TID)	High Dose Rate (HDR)	40 krad(Si)	30 krad(Si)
	Low Dose Rate (LDR)	40 krad(Si)	30 krad(Si)
Single-Event Effects (SEE)	Destructive (SEB, SEGR, SEL)	Not applicable	≥ 42 MeV/mg/cm <sup>2</sup>
	Non-Destructive (SET, SEU, SEFI)	Not applicable	≥ 30 MeV/mg/cm <sup>2</sup>

### 6.5.2 RHA Plan Summary

Test	RHA Plan for VSC Series DC-DC Converters
Total Ionizing Dose (TID):	Sensitive semiconductor components undergo RLAT to 40 krad(Si) per MIL-STD-883 Method 1019. Converters are characterized to 30 krad(Si).
Enhanced Low Dose Rate Sensitivity (ELDRS):	Converters were tested at 10 - 100 mrad(Si)/s up to 40 krad(Si). Converters are characterized to 30 krad(Si).
Single Event Effects (SEE):	Converters are characterized to LET ≥ 42 MeV/mg/cm <sup>2</sup> for catastrophic events (SEL, SEB, SEGR) and to LET ≥ 30 MeV/mg/cm <sup>2</sup> for transients (SET) and functional interrupts (SEFI) under heavy ion exposure.
Radiation Lot Acceptance Testing (RLAT):	All production lots of sensitive semiconductor components undergo a sample test for TID at HDR or LDR.

## 7.0 ENVIRONMENTAL SCREENING

Test	/ES+
Internal Visual	IPC-A-610, Class 3
Temperature Cycling	MIL-STD-883, Method 1010, Condition B, -55 °C to +125 °C, 10 Cycles
Burn In	96 hours at +105 °C
Final Electrical	-55 °C, 25 °C, 105 °C <sup>1</sup>
External Visual	Internal Procedure

1. 100% R&R testing with all test data included in product shipment

## 8.0 ORDERING INFORMATION

VSCPL	12	10	S	G	/ES+
1	2	3	4	5	6

(1) Product Series	(2) Nominal Input Voltage	(3) Output Current	(4) Number of Outputs	(5) Package Option	(6) Screening Code
VSCPL	12 12 Volts	10 10 Amps	S Single	G Gullwing	/ES+

Please contact your sales representative or the VPT Inc. Sales Department for more information concerning additional environmental screening and testing, different input voltage, output voltage, power requirements, and source inspection.

## 9.0 CONTACT INFORMATION

To request a quotation or place orders please contact your sales representative or the VPT, Inc. Sales Department at:

**Phone:** (425) 353-3010  
**Fax:** (425) 353-4030  
**E-mail:** [vptsales@vptpower.com](mailto:vptsales@vptpower.com)

All information contained in this datasheet is believed to be accurate, however, no responsibility is assumed for possible errors or omissions. The products or specifications contained herein are subject to change without notice.

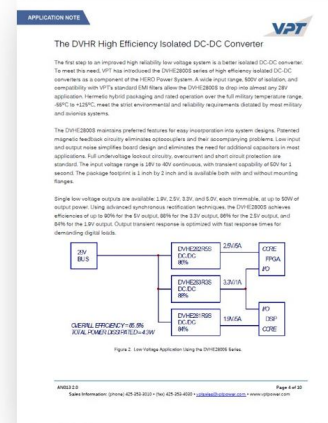
## 10.0 ADDITIONAL INFORMATION

Visit the VPT website for additional technical resources, including:

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